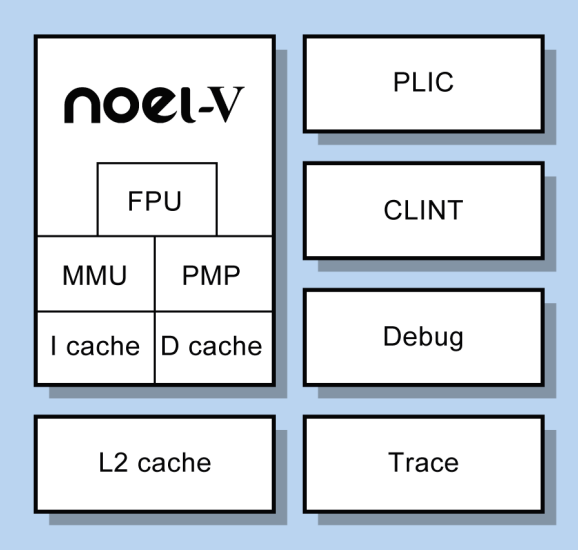
PRODUCT BRIEF

RISC-V PROCESSOR IP CORE

NOEL-V

Highly configurable RISC-V processor

- Suitable for both FPGA and ASIC
- Optional fault-tolerant features for space applications
- Multi core support (SMP/AMP)
- 32-bit or 64-bit architecture
- Dual-issue, in-order, 7-stage pipeline
- Hypervisor extension for virtualization
- Native AMBA 2.0 AHB bus interface
- Subsystem including L2 cache with AHB or AXI backend also available
- Area efficient or high performance FPU



NOEL-V provides unmatched flexibility and customization options, empowering SoC designers to create tailored solutions that perfectly meet their unique requirements. The table below showcases some example configurations, available in both 32- and 64-bit architectures. It's also possible to finely customize more configurations. Moreover, fault-tolerant features can be enabled for all configurations.

CONFIG.	TARGET	PIPELINE	RISC-V EXTENSIONS	MMU	PMP	PRIVILEGE MODES	EXAMPLE SOFTWARE
HP	High performance	Dual issue	IMAFDCHB*	Yes	Yes	Supervisor, User and Machine + Virtualization	Hypervisor, Linux, VxWorks
GP	General Purpose	Dual or single issue	IMAFDCHB*	Yes	Yes	Supervisor, User and Machine + Virtualization	Hypervisor, Linux, VxWorks
GP-lite	General purpose Area optimized	Dual or single issue	IMAFDCB*	Yes	No	Supervisor, User and Machine	Linux, VxWorks
MC	Controller applications	Single issue	IMAFDCB*	No	Yes	User and Machine	RTEMS
MC-lite	Controller applications Area Optimized	Single issue	IMA	No	No	User and Machine	RTEMS

*Only the currently ratified parts of B (Zba, Zbb, Zbc and Zbs) are implemented. Several other ratified extensions, such as Zbkx, Zicbom, Zfh, Sscofpmf and Sstc are also implemented.

RISC-V Extensions:

I – Base Integer instructions
M – Hardware support for Multiply and Division
A – Atomics
FD – Single/Double Floating Point
C – Compressed (16 bits) instructions
H – Hardware hypervisor support
B – Bit Manipulation support

RELEASED MARCH 2023

PRODUCT BRIEF

RISC-V PROCESSOR IP CORE

NOEL-V

The NOEL-V processor model implements open standards developed within RISC-V International and allows SoC designers to leverage the peripherals and example designs that are provided with the GRLIB IP library. The NOEL-V can run complex operative systems providing performance comparable to an ARM Cortex A53.

Synthesis

The NOEL-V processor can be synthesized with common commercial synthesis tools. The processor model is highly portable between different implementation technologies. The processor is delivered with example designs for many common boards and FPGA technologies.

Software development

The NOEL-V processor implements the RISC-V ISA which means that compilers and kernels for RISC-V can be used with NOEL-V (kernels will need a NOEL-V BSP). To simplify software development, we provide several prebuilt toolchains.

Fault tolerance

The processor core is also available in a fault-tolerant version where on-chip memories are protected against radiation effects and where radiation induced errors are handled without software interruptions.

Architecture

In its most performant configuration, the NOEL-V is implemented as a dual-issue processor, allowing up to two instructions per cycle to be executed in parallel. To support the instruction issue rate of the pipeline, the NOEL-V has advanced branch prediction capabilities.
The write-through Level-1 cache has a wide bus interface, supporting fast cacheline fills, and a store-buffer.

Availability

The NOEL-V is immediately available.
A version without the pipelined FPU and without fault-tolerance features is part of the free open source GRLIB library (see gaisler.com/getgrlib).
Prebuilt evaluation bitstreams are available for FPGA development boards.

Please see **gaisler.com/NOEL-V** for additional information.

RELEASED MARCH 2023